AMENDMENTS TO THE CLAIMS

1-27. (canceled)

28. (previously presented) A method of determining a value of a resistance in a circuit comprising steps of:

discharging a capacitance through the resistance while repeatedly recharging the capacitance, said recharging being performed with a pulsing recharging signal;

determining a duty cycle of the recharging signal; and

obtaining the value of the resistance from the duty cycle of the recharging signal.

29. (previously presented) A method of determining a value of a resistance as in claim 28, wherein the recharging signal for the capacitance is a substantially constant current.

30. (previously presented) A method of determining a value of a resistance as in claim 28, wherein the recharging signal is pulsed, and the duty cycle is determined by counting recharging signal pulses during a sensing period.

31. (previously presented) A method of determining a value of a resistance as in claim 30, wherein the capacitor is charged prior to a start of the sensing period.

32. (previously presented) A method of determining a value of a resistance as in claim 30, wherein the circuit includes a resistance-based memory.

33. (previously presented) A method of determining a value of a resistance as in claim 32, wherein the resistance-based memory is an MRAM.

Claims 34-37. (canceled)

38. (previously presented) A method for sensing a value of a resistance comprising:

charging a capacitance to a voltage level above a threshold value;

selecting one of a plurality of resistances;

discharging the capacitance through the selected resistance;

generating at least one recharging pulse each time the voltage level on the capacitor falls below the threshold value;

using the recharging pulse to recharge the voltage level on the capacitor above the threshold value; and

determining a reference value of the selected resistance from the number of recharging pulses which are generated during a finite period of time during which the capacitance is discharging through the selected resistance.

39. (previously presented) A method as defined in claim 38 wherein the discharging includes discharging the capacitance through the resistance at a constant current.

Claims 40-51. (canceled)

52. (currently amended) A device state sensing circuit comprising:

a ~~controlled~~ voltage supply;

an electronic charge ~~reservoir~~ storage device electrically connected with the ~~controlled~~ voltage supply;

a current source electrically connected with the electronic charge reservoir; and

a pulse counter in communication with the current source to generate a pulse counter count;

wherein the ~~controlled~~ voltage supply is operatively connected to a selected memory cell of a memory device comprising a plurality of memory cells to maintain a substantially constant voltage across a resistive element of the selected memory cell;

the electronic charge reservoir is operatively connected to the ~~controlled~~ voltage supply to provide a current through the resistive element;

the current source is operatively connected to the charge reservoir to repeatedly supply a pulse of current to recharge the charge reservoir upon a predetermined depletion of electronic charge from the reservoir through the resistive element; and

the pulse counter count is a number of the pulses supplied by the current source over a finite time period during which the current is supplied through the resistive element, the ~~contents of the~~ pulse counter <u>count</u> representing a logic state of the selected memory cell.